Research on Wireless MIL-STD-1553B Bus Based on Infrared Technology

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Abstract—Infrared technology has the benefits of low mass, size, power and cost, minimum electromagnetic interference (EMI), efficient and reliable data transfer, which is suitable for the communications in small spacecrafts. A wireless data bus system based on infrared technology for intra-spacecraft communication is proposed in this paper. The bus protocol is following the traditional MIL-STD-1553B, while the 1553B bus transceivers, transformers and cables in the physical layer are replaced by infrared transceivers. Infrared transceivers shouldn't affect the 1533B higher layers and the layout of the onboard equipment. So a wireless bus is designed via diffuse optical wireless links. This paper focuses on the implementation of an IR wireless 1553B bus system, including hardware design of the wireless bus nodes, logic design of the 1553B bus protocol on FPGA, and the signal formatting between 1553B signals and IR signals. A radiation-hard application specific integrated circuit (ASIC) chip is designed for the application of the wireless 1553B bus in future space missions. Experimental results prove the reliability and feasibility of the wireless data bus system. Finally, some challenges and problems in space applications are put forward.

Index Terms—MIL-STD-1553B; Infrared Communication; Wireless Bus; Intra-Spacecraft; FPGA

I. INTRODUCTION

Nanosatellites operating singly or in clusters will account for a place in future space missions. Communication buses within spacecrafts require relatively large, heavy, custom-designed wire harnesses which have greatly limited the development of small satellites. In recent years, wireless communication technologies have drawn great interest from the space agencies all over the world, such as NASA, ESA, CCSDS (the consultative committee for space data system) [1, 2], etc. Compared with radio frequency (RF) technologies, the most advantage of infrared technology is electromagnetic interference/compatibility (EMI/EMC), which will reduce the effect to other electronic devices and ease the technology insertion. Therefore, infrared technology is a promising technology to solve the problems caused by the wire harnesses for small spacecrafts.

The national institute for aerospace technique (INTA, Spain) [3, 4] has a ten-year research history on optical wireless links to intra-spacecraft communications (OWLS) and has achieved abundant experience and results in the field. Several wireless applications were carried out in representative scenarios at ground level, and in-flight experiments. An optical SPI bus, the first in-orbit experiment of OWLS was carried out in NANOSSAT-01 satellite which was developed by INTA and launched in 2004 onboard Ariane V as a secondary payload of the Helios1B satellite. Also, a wireless CAN bus via infrared technology was demonstrated in satellite FOTON-M3 in 2010.

Studies on wireless technologies for intra-spacecraft communications began in 2009 in China [5-7]. Studies on wireless technologies for space missions need the support of continuous and serial programs and plans. This work was sponsored by Space Science Strategic Leading Technology Specials of the Chinese Academy of Sciences. The Center for Space Science and Applied Research (CSSAR) and the Shanghai Institute of Microsystem and Information Technology (SIMIT) took part in this work. The CSSAR focused on the development of an infrared intra-spacecraft bus demonstrator and the SIMIT focused on the optical energy transmission analysis and testing in several representative spacecraft environments. In this paper, implementation of an infrared 1553B data bus system for intra-spacecraft communication is proposed in detail and a radiation-hard ASIC is designed for future space applications. At last, some experimental results are presented to verify the feasibility of the wireless bus system.

II. REVIEW OF 1553B BUS AND INFRARED TECHNOLOGY

MIL-STD-1553B is a command-response asynchronous serial data bus. The principal characteristics are distributed processing, centralized control and real-time response. Because of its excellent performances, 1553B bus is widely used in aviation, spaceflight, navigation and some weapons.

1553B bus adopts dually redundant bus topological structure for reliable communication, excellent fault tolerance and fault isolation. There is only one active bus controller node (BC), up to 30 slave or remote terminal nodes (RT), and one monitor node in 1553B bus. All communications in 1553B bus are initiated by one or more BC command. Data words and all non-broadcast RT responses are preceded by a status word. Communication nodes at the physical layer can be direct or transformer coupled in 1553B bus. As the transformer coupled mode can provide DC isolation, it is the most...
usual and typical mode in 1553B bus. 1553B bus is typically a copper bus consisting of twisted-shield-pair wiring. The data rate of 1553B bus is 1 Mbps, and data encoding is Manchester II bi-phase level encoding.

Implementation of 1553B bus can be realized in two ways. One is to use 1553B bus protocol chips (BU-65170/61580, COM1553B, UT1553B) to design 1553B bus interface, and the other way is to buy and implant 1553B protocol IP core (DDC’s 1553B Core, Condor’s Core-1553B, Actel’s Core1553BRT) into FPGA. The two hardware design methods can be unified, as shown in “Fig. 1,” including one microprocessor, 1553B protocol chip, 1553B transceiver, 1553B transformers, power supply and other peripheral circuits. The 1553B protocol chip can be replaced with an FPGA with 1553B IP core. Some integrated chips contain both 1553B protocol and 1553B transceiver, such as BU-61585. The mass, size and power of 1553B bus interface circuit are well-known large. For example, 1.7 W is needed per transmitted word for one 1553B transceiver and 0.55 W is needed in quiescent mode according to the BU-61585 datasheet (reference [8]). In recent years, 1553B chips used in China have been seriously depended on foreign manufacturers, which is bad for the continual development of Chinese space and defend missions.

Light-Emitting Diodes (LEDs) using for free-space communication is well known and mature in the field of infrared remote controls and low-speed links standardized by the Infrared Data Association (IrDA) between electronic equipments. There are up to 4Mbps link speed components in the IrDA specification, and higher speed components are under developing. Unfortunately, IrDA is targeted to very short range. The IrDA physical specification only requires 1m operation range and minimum 30 degrees beam width at approximately 875nm [9]. Most existing available components exceed this specification. Relevant experiments with LEDs [10-11] such as high speed communications, useful lifetime, optical networking, modulation and demodulation, can be helpful in this work.

Infrared transceivers shouldn’t affect the 1553B higher layers and the layout of the onboard equipments, so the design of the infrared diffuse reflection is adopted. Because 1553B data rate is 1 Mbps and Manchester coding is used, the least 1553B pulse width is 500ns. For the low power consideration, infrared pulse width should be as short as possible. The Infrared Data Association (IrDA) regulates different infrared data rates of which the high speed mode 4Mbps is suitable for 1553B bus signals. Therefore, 4Mbps infrared transceivers are selected for this wireless 1553B bus. Although the data rate is 4Mbps, the actual pulse width of the IR transceivers is 125ns to distinguish continuous logic 1. Therefore, it’s necessary to format signals between 1553B signals and IR signals.

This paper focused on the implementation of an IR wireless 1553B bus system including hardware design of the wireless bus nodes, logic design of the 1553B bus protocol on FPGA, the signal formatting between 1553B signals and IR signals and design of a Rad-hard ASIC.

### A. Hardware Design of the IR 1553B Bus Nodes

There are three kinds of nodes in 1553B bus, BC, RT and MT. The hardware design of the three nodes can be the same, and functional differences can be realized by CPU software. The hardware design of 1553B bus nodes based on infrared transceivers is illustrated in Fig. 2. There is a microprocessor to control data communication, a FPGA to realize the 1553B protocol logic and the formatting between 1553B signals and IR signals, infrared transceivers to transmit and receive pulses via infrared, power supply and other peripheral functions. The embedded microprocessor in the FPGA that can take the place of the single chip microprocessor will make the node hardware even easier and smaller. This method is a very popular technology called SOPC (System On Programmable Chip) now. But on account of the harsh space environment, a radiation-hard ASIC should be designed in the long run to make infrared communication possible in space.

Infrared transceivers can be integrated IR chips or discrete components. The integrated IR chips generally contain LED, photodiode transducer, LED driver, modulation and demodulation, amplifier circuit, etc. The integrated IR chips are simple to interface digital chips and easy to use, which makes it widely used in the ground tests and demonstrators. But in the later space applications, it is necessary to use Rad-Hard components [11] to design IR transceivers.

When the traditional 1553B bus controller transmit one bit, it takes 1000ns. But it is only a 125ns pulse in the IR 1553B bus mode, which means that the total duty cycle of the IR mode is 0.125. The peak current of an IR transceiver working in the transmitting mode is usually 650mA. If the IR transceiver working voltage is 3.3 V, the average power consumption of the transmitting node is $650 \times 3.3 \times 0.125 = 270\text{mW}$, which is much less than traditional 1553B transceivers.

Compared with the hardware design of a traditional 1553B bus, the hardware design of the IR wireless 1553B bus nodes in this paper has much less power consumption.
size and mass, which is quite fit for small and nano satellites.

![Hardware design of 1553B bus based on infrared](image)

**B. 1553B Protocol IP Core**

The design of 1553B protocol IP core is important to the development of Chinese defense and space industry. The 1553B IP core in this paper has been fully tested and verified, and has detailed design documents, full test benches, and good reconfiguration feature, in order to reuse in different designs. The 1553B protocol IP core can be implanted in a FPGA, ASIC or SOPC, which is a low-mass, low-size, and low-power solution for the implementation of 1553B bus.

The architecture of 1553B protocol IP core is illustrated in Fig. 3. This IP core consists of BC function block, RT function block, CPU interface, system registers, RAM arbitrator, shared RAM, channel multiplexer, Manchester encoders, Manchester decoders, output Mux and a timer. The IP core can be configured to work as a BC or a RT. As BC and RT functional block won’t work simultaneously in one 1553B IP core module, the two blocks can share the other resources in the IP core. The internal registers and memory need to be configured by CPU via the CPU interface before the IP core begins to work. One of the particular designs for the space SEU (single event upset) is that the shared RAM (4k bytes) adopts ECC check (Error Correction Code) which can correct one error and detect two errors. If SEU happens, an interrupt request will be sent to the CPU. CPU will handle the request, correct the error and record the event.

The IP core can be configured to work in the traditional 1553B mode or IR 1553B mode by CPU. Meanwhile, corresponding external transceivers are needed to realize 1553B data transfer. For example, a traditional 1553B transceiver and two transformers are needed when the IP core is configured to work in the traditional mode by CPU. IR transceivers are required if the IP core works in the IR 1553B mode.

CPU can command and control the 1553B IP core by operating the internal registers via the CPU interface. Intel demultiplexed access timing is adopted in the CPU interface module. The internal registers include the configure register (CR), interrupt status register (ISR), time tag register, frame-start register, frame-stop register, interrupt erase register, and so on. The timer is a 16-bit counter to provide system time for the 1553B node.

The BC module can be configured to work in a single frame or frame auto-repeat operation by the CPU. The inter-message gap and frame timing can be programmed by the CPU. There is a descriptor stack that records all messages in one frame that BC is ready to send out to the RTs. The descriptor stack can record up to 38 messages. These messages’ control information is in the descriptor stack, such as command words, message control word, transmit/receive address pointer, etc. BC module has a state machine at the top level that controls the message flow, as shown in Fig. 5. Once the frame-start register is high, the state machine starts to work. It reads the descriptor stack to get message information. In the “command analysis” state, the state machine decides the next state according to the command word read from descriptor stack. After the message is over, the state machine will detect if the frame-stop register is valid to decide if the frame will go on. The function of the BC message handling state (such as RT-receive state, RT-to-RT state, etc.) is basically memory control.
The RT module has a command illegalizing table, a sub-address control word look-up table, and a message description stack. The command illegalizing table enables the RT to check the received command from the bus, if the word count/mode code doesn’t match the definition in the illegalizing table, this command will be ignored. The sub-address control work look-up table defines the information of every receive/transmit sub-address, such as interrupt enable-bit, receive/transmit address pointer, circular buffer mode enable bit. The message description stack records the received messages’ information for CPU to lookup. Single message mode and circular buffer mode are available for the RT subaddresses, which can be realized via configuring sub-address control work look-up table by CPU.

The RT works under the control of the RT module state machine shown in Fig. 6. After the state machine receives a command word from the decoder block, it first checks if this command word is legal for itself by reading the command illegalizing table and the sub-address control word look-up table. If the command is a legal receive command, RT waits the data words and saves them to the receive RAM. After receiving the data words according to the command word, RT wait for a couple microseconds, then transmit a status word that recording the RT operating status to BC. At last, RT records this command and corresponding information in the RT description stack. Similarly, RT deals with the other commands. CPU can operate RT by enabling RT interrupt.

As BC and RT functional block won’t work simultaneously in one 1553B IP core module, the descriptor stack of the BC block shares the same memory with the command illegalizing table, the sub-address control word look-up table, and the message description stack of the RT block to save system memory of the IP core.

The Manchester decoder and encoder module are very important to the 1553B IP core, because they are the basis of the other blocks. If the decoder module can’t decode the data correctly, the 1553B IP core can’t get the information from the bus and the IP core design will make no sense. The input of the decoder module is synchronized by the decode clock before it enters the decode state machine. After detecting the effective sync signals of the 1553B word, the synchronized input is directed to a state machine to decode. According to the signal format of the 1553B bus shown in Fig. 7, there are four effective signal states for the decoder state machine to judge. Counters are used to distinguish the four states. 16MHz clock is used to sample the input signal, so every data bit (1us) in 1553B bus has 16 clocks, and the sample signal of the first 8 clocks is converse with the latter 8 clocks. For example, after the decoder state machine
detected a low level pulse of 1.5us, it detected a high level pulse of 0.5us, then the state machine judged that the 15th bit of this word was logic 1. Because there is one of the four effective conditions in 1553B bus signals. The state machine continues to decode the signals according to the Manchester code. Similarly, the decoder can recognize and decode the words in the other conditions. The design of the decoder is tested and verified by module simulation and FPGA, and the error rate of the decoder is lower than 10^{-10}.

Three external transceivers are available for the 1553B IP core: the traditional 1553B transceiver (HI-1568 from HOLT, etc.), RS485 transceivers (55LBC176 from TI, SP481E from SIPEX, etc.), and 4Mbps infrared transceivers (HSDL3600 from Agilent). The output mux module is controlled by the internal registers to select the right signals for external transceivers.

C. Signal Formatting Between 1553B and IR

The signal formatting logic between 1553B and IR signals locates in the output mux module. IrDA suggests the high speed mode 4Mbps modulated by 4-PPM, which requires phase-locking using a phasing preamble. An asynchronous unipolar return-to-zero (RZ) modulation scheme which is much easier in practice is used in this design.

1553B pulse train from the 1553B encoder module needs to be formatted into 125ns IR pulse by 16MHz before it outputs to the IR transceiver, as shown in Fig. 6. 1553B pulse train is sampled by 2MHz clock. If the 1553B signal is high, a 125ns pulse will be generated. It is simple to realize the sampling logic in FPGA.

The IR pulse to 1553B formatting uses the pipeline and combinational logic. The pipelined IR signals by 16MHz clock first make the logical AND, then get into the Manchester decoder module. Test and verification results by simulation and FPGA implementation prove the validity of this module design.

D. Design of a Rad-Hard ASIC

Considering the harsh space environment, a radiation-hard ASIC is designed to make infrared communication possible in space. The system architecture of the ASIC named WH1771 is shown in Fig. 8, including a logson CPU, a 1553B protocol IP core and formatting logic between 1553B and IR signals to realize an IR wireless 1553B bus. This ASIC [13] has been available now for space missions.

A technology demonstrator is designed to test the wireless 1553B bus based on infrared technology. The demonstrator shown in Fig. 7, contains a PC with DDC’s PCI 1553B test card, a FPGA, a 1553B bus transceiver and infrared transceivers. Integrated IR chips HSDL-3600 are used in this demonstrator for node simplicity. The 1553B bus transceiver HI-1568 is used to test the design of 1553B protocol IP core. HSDL-3600 is a low-profile infrared transceiver module that provides interface between logic circuits and IR signals for through-air, serial, half-duplex IR data link. HSDL-3600 contains a high-speed and high-efficiency 870nm LED, a silicon PIN diode, and an integrated circuit. Its high speed mode 4Mbps fits the demand of an IR wireless 1553B bus. The hardware design of HSDL-3600 is illustrated in Fig. 8, in which the capacitor C32, C33 should be placed within 0.7cm of the HSDL-3600 to obtain optimum noise immunity.

The design of 1533B IP core will directly influence the performances of a wireless 1553B bus. In the test of 1553B protocol IP core, more than 10^7 messages have been tested. There is no parity error or Manchester error in the tests. The bit error of the 1553B IP core is smaller than 10^{-9}.
Fig. 12 shows the simulation wave of a BC-to-RT message via infrared transceivers. BC sends a command word “0021” to let the RT to receive a data word “0001” in subaddress “1”. In Fig. 12, “busp_ta” and “busn_ta” of the BC node are from the Manchester encoder module to the output_sel module and signal “busp_ta0” is the formatted output to the IR transceiver. The RT node receives the signal “busp_ra0” from IR transceiver and format it to 1553B signal “busp_ra_ir”, “busp_ra_ir” is decoded as the command word “0021” and the data word “0001” by the decoder. After the analysis of the command word, RT node send its response, the status word “0000”, to BC. Fig. 13 shows the simulation wave of a RT-to-BC message via infrared signals. BC sends a command word “0421” to let the RT to send a data word in subaddress “1”. After receiving and decoding the command word, RT sends out a status word “0000” and a data word “0100” to BC via infrared signals according to 1553B bus protocol.

Fig. 14 shows that the FPGA output a formatted 1553B signal for the infrared transceiver in the BC node, which verified the design of the signal formatting between 1553B signal and infrared signal.

V. CONCLUSIONS

The demonstrator tests prove the feasibility of the wireless 1553B bus system based on infrared technology. However there are some challenges and problems in space applications for a IR wireless 1553B bus, for example Rad-Hard infrared components, limited communication distances, different material characteristic of satellite structures, etc. The IR wireless 1553B bus is a potential low-mass, low-size, low-power and low-cost solution for the implementation of 1553B bus, which is quite fit for small and nano satellites. This warrants further, more detailed investigation in China [14].

ACKNOWLEDGMENT

The authors wish to thank the Chinese Academy of Sciences. This work was supported by Space Science Strategic Leading Technology Specials of the Chinese Academy of Sciences under Grant XDA04070000.

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