

A Fully-Integrated Buck Converter Design and Implementation for On-Chip Power Supplies

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Abstract—A 5V-2.5V fully-integrated low-power buck converter was designed and implemented using 0.5 μ m CMOS technology. The critical circuits of the high frequency controller and an on-chip multi-layer spiral inductor were presented. The structure of multi-layer spiral inductor having parallel and series branches of the metal strip. As the result that the parallel branching structure greatly reduced the series resistance and the series branching structure greatly improved the series inductance of the inductor, the structure can achieve quality factor and current capability enhancement while compatible with conventional CMOS process. The quality factor was quantitatively analyzed with a scalable model and its origin was investigated at a structural point of view. From chip measurement results, when the converter is running at the rated load, the average output voltage of 2.5V, the output voltage ripple within $\pm 2\%$, and the energy efficiency of 46% are achieved.

Index Terms—fully-integrated buck converter, spiral inductor, output voltage ripple, fourth term, energy efficiency

I. INTRODUCTION

With the developing of the CMOS technology, CMOS digital logic and analog signal processing is integrated into system-on-a-chip (SOC). As these integrated circuits are scaled to deep submicron dimensions, internal switching frequencies become several orders of magnitude faster than off-chip signals and external power supplies and control logic are incapable of responding to load conditions without significant delay [1]. Therefore, a monolithic power supply circuit including both active and passive elements must be integrated on the chip to meet the size and weight restrictions and improve the power conditions.

Manufacturing on-chip inductors of high quality factor (Q) in a commercial CMOS technology is still a challenge, especially for the large inductance about tens nanohenries required in dc-dc converters. In the recent years, a large amount of modeling, characterization, and design work has been done to study air-core spiral inductors on silicon technology for both radio-frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs). In order to improve the quality (Q) factor of the spiral inductors, many researches focus on the multi-layer structure, such as series stacked

structure increasing the inductance value due to the mutual magnetic coupling [2], and double or multiple shunt structure dropping the series resistance [3, 4]. However, for the spiral inductors used in fully integrated DC-DC converter, the simply series or shunt connection multilayer structure fabricated in conventional CMOS silicon process is difficult to satisfy the desired Q value, current capability and the limited of the occupied area directly [5].

In the present paper we designed a series parallel spiral structure on silicon to enhance Q value, inductance per unit area and current capability. In the considered CSMC mix-signal 0.5 μ m 2P3M CMOS technology, the top metal M3 is the thickest and usually double times than other metals. Based on this fact we designed a multi-layer spiral inductor which M3 series with the shunt-wound M2-M1, and presented a scalable SPICE compatible lumped element equivalent circuit model for DC-DC converters operating at hundreds mega-hertz. From the measurement results, the designed inductor allows alignment of its peak quality factor to the circuit's operating frequency. The model agrees well with measurements with the interesting frequency, from 50MHz to 500MHz. This model provides a method of custom multi-layer spiral inductor design for fully integrated DC-DC converters prior to fabrication.

To reduce the size of the components, high operation frequency of 100MHz were applied. However, the control system will be unstable at high frequency [6]. Therefore, the emphasis of this work is the design of steady control system and the physical design of multi-layer spiral inductor.

As an example, a 5V to 2.5V fully-integrated buck converter including on-chip passive components has been designed and presented in this paper. The block diagram of the buck converter with its control circuit is shown in Fig.1. During the pass device M_1 is on, the current flowing through the inductor rises. As the switch M_1 turns off and rectifier M_2 turns on, the inductor induces a negative value of the voltage. The current in the inductor decreases and the energy stored in the inductor is delivered to the load.

The organization of the paper is as follows. First, in section II, outlines the main circuits designed in

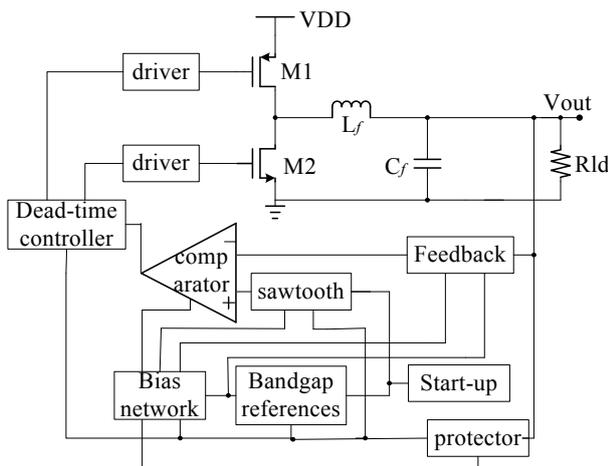


Figure 1. Circuit schematic of the buck converter. Pass device M1, rectifier M2, on-chip filter inductor and capacitor L_f, C_f constitutes the main circuits. The others make of the controller.

controller. Then, section III describes the physical design, modeling and measurement results of multi-layer spiral planar inductor. Then the simulation and measurement results of overall buck converter is reported in section IV. Finally, section V is conclusions.

II. DESIGN OF CONTROL CIRCUITS

The control circuit is designed specially for the fully integrated buck converter that is capable of operating at high frequency with lower-power dissipation. The circuit block diagram is shown in Fig.1, which is composed of sawtooth wave generator, comparator, feedback circuit, start-up block, protection circuit, band-gap references, bias network, dead-time controller and MOSFET drivers. The duty cycle is modulated by the PWM controller to maintain the output voltage at the desired value whenever variations in the load current and input supply voltage are detected. The key circuits of Op-amps, comparator, and feedback compensation network are described in this paper.

A. Operational Amplifier

The operational amplifier is the kernel of the feedback control network. Because the switching frequency of buck converter is as high as 100MHz, the bandwidth must be over 100MHz to cover the high switching frequency of the converter. A folded cascode operational amplifier [7] is used in this design, shown in Fig. 2. In this circuit, the chosen of the bias current I_3, I_4 and I_5 must be seriously to avoid the dc current in cascode current mirror equals to zero, $I_4=I_5=1.25I_3$ is applied in this design.

By the simulation, the unity-gain bandwidth is located at 195MHz with phase margin of 68° . The open loop dc gain is 66dB, and the power dissipation is about 2.3mW.

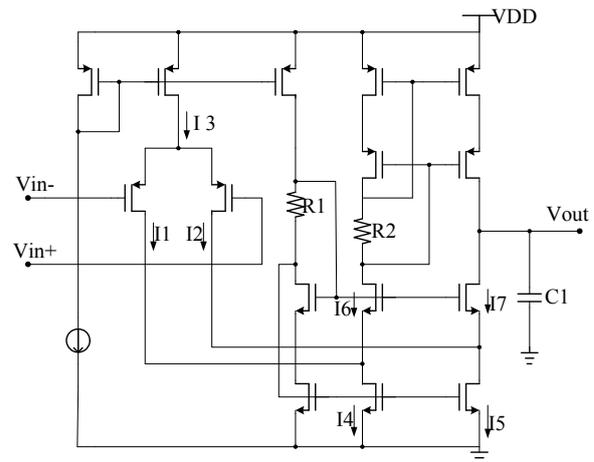


Figure 2. Operational amplifier circuit.

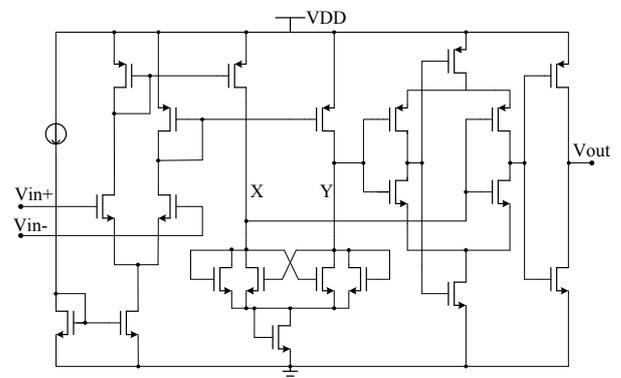


Figure 3. Comparator circuit.

B. Comparator

Comparator decides the comparative accuracy between the reference voltage and the output voltage of sawtooth waveform generator, as well as the accuracy of the duty cycle. The circuit of comparator is shown in Fig. 3, including a preamplifier, positive feedback circuit and output buffer.

In preamplifier circuits, input signal is amplified to increase the accuracy of the comparator, and the switch noise made by input signal is kept away from the positive feedback circuit. Positive feedback circuit is the core of comparator. It can identify the signal of a few mV.

By the simulation results, transfer delay is 2.3ns, comparison accuracy is 1.8mV, and power loss is 3.3mW. It shows a good behavior in the designed feedback control loop.

C. Compensator

In control circuit, it is necessary to design a compensation network for ensuring the relative stability, the line rejection and load rejection and the fastness of the transient responses. The double-poles and double-zeroes compensator network is designed for achieving the

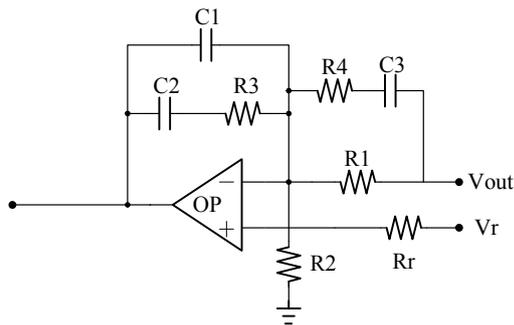


Figure 4. Compensator circuit.

best transient response. Fig. 4 shows the circuit. The minimum phase margin is designed to have 45°.

III. THE PLANAR INDUCTOR DESIGN IN A BUCK CONVERTER

In a CCM buck converter, the filter inductance L_f is defined using expression [8]

$$L_f = [V_{out}(1-D)] / (\Delta i_{p-p} f_s) \quad (1)$$

where duty cycle D is define as $D=V_{out} / V_{in}$, V_{in} and V_{out} are input and output voltage respectively, Δi_{p-p} is the inductor current peak-to-peak value, ΔV_{out} is the output voltage ripple, f_s is the switching frequency. From this equation, the required inductance is in inverse proportion to the f_s and Δi_{p-p} when the rated input and output voltage are decided.

By increasing the f_s and Δi_{p-p} , the less inductance is required in DC-DC converters and the physical structure of on-chip spiral inductor can be achieved more easily too. However, the chosen of the both value could not be as high as possible because of the following reasons. First, the switching power dissipation of the synchronous switching transistors in a DC-DC converter increase with the increasing switching frequency, thus decreased the conversion efficiency of the system. Then, by choosing a higher current ripple Δi_{p-p} , a lower filter inductance can be achieved. However, the metal strip width must be large enough to handle this ripple current and the parasitic capacitance and inductance per unit area is very metal width dependent in the multi-layer structures, the poor quality factor and high cost will be obtained when the metal width is above certain value. Therefore, the tradeoffs among these factors must be considered.

A. Physical Design

In a standard CMOS technology, the top metal is usually the thickest and about double thickness than other metals. It also indicates that the current handling capability of the top metal is double than other metals with the fixed metal width. As a result, the current handling capability of the simple series multi-layer spiral inductors is limited by the lower metal strip. To achieve the inexpensive noninvasive process-independent complete silicon integration, a series parallel multi-layer structure was designed in this study as shown in Fig.5.

TABLE I.
PARAMETERS SPECIFICATION OF THE USED TECHNOLOGY

$R_s(\Omega\text{-cm})$	Metal thickness (μm)		SiO_2 thickness (μm)
	Lower	Upper	
20	0.6	1.1	1.05

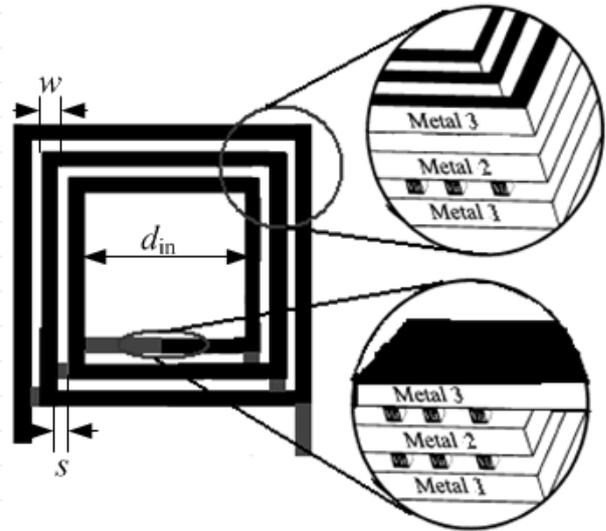


Figure 5 Series parallel stacked inductor

Using CSMC mix-signal 0.5- μm 2P3M CMOS technology specified in Table I we designed the structure of the shunted M1-M2 series with M3. The effective thickness of the shunted M1 and M2 can be considered as the sum of their thickness because the vias between them are arrayed with proportional spacing.

B. Modeling

When stacking metal layers to obtain thicker conductor and a higher inductance in unit area, the complexity must be fully understood to achieve optimum Q . The simplest approach taken in the new model is to break the inductor

into segments, as seen in Fig.6. Each element of the model is based on the physical attributes of the inductor and process stack, therefore, the parasitic elements are calculated from the principles in [9] and the inductance is calculated using the data fitted monomial expression in [10] for the advantage of the optimization. However, this distributed model is not suit to the DC-DC circuit simulation and inductors Q optimization. As the result, the lumped model for the inductors optimization and circuit simulation is educed in the following.

First, the calculation of the total inductance of the designed structure must be considered seriously. For the shunted M2-M1, the two spirals had the same dimension parameters, and the contact vias between them were

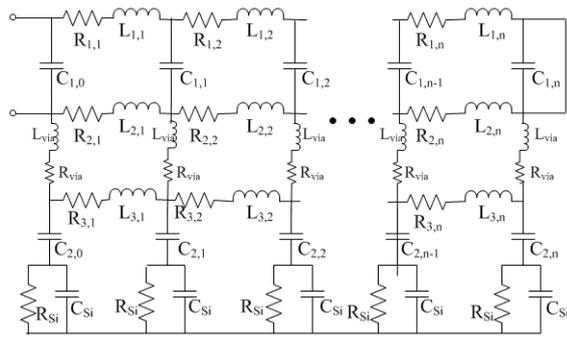


Figure 6 The distributed model of the designed spiral inductor

uniformly distributed as shown in Fig.1. Thus, we can neglect the total vias inductance L_{via} and total vias resistance R_{via} and consider that the mutual coupling between the two layers is quite strong and can obtain the following relationship,

$$L_{s12} = L_{s1} = L_{s2} \quad . \quad (2)$$

The shunt M1-M2 then series with M3 and the total inductance of a series parallel spiral is

$$L_s = L_{s3} + L_{s12} + 2M_{23} \quad . \quad (3)$$

The inductance of the coil in each layer L_n is expressed as below [10],

$$L_n = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad (4)$$

And M_{23} is the mutual inductance between M3 and shunted M2-M1, it can be obtained using the expressions in the [11].

The series resistance of the each spiral is same as the expression in[6],

$$R_{sn} = \rho \cdot l / \left[w \cdot \delta \cdot \left(1 - e^{-l/\delta} \right) \right] \quad (5)$$

and the total resistance of this structure is simple

$$R_s = R_{s1} // R_{s2} + R_{s3} \quad . \quad (6)$$

The next important element in the designed structure which different from the conventional structure is the series capacitance. In this series parallel spiral inductor, since the adjacent turns of shunted M2-M1 can be considered as almost equipotential, the crosstalk capacitance among them can be negligible. However, the parasitic capacitance due to the overlap between the M3 and shunted M2-M1 is significant, which is equal to

$$C_s = lw\epsilon_{ox} / t_{ox,3} \quad . \quad (7)$$

where l is total metal length of each spiral, w is metal width, ϵ_{ox} and $t_{ox,3}$ are the dielectric coefficient and thickness of the SiO_2 layer between M3 and M2 respectively.

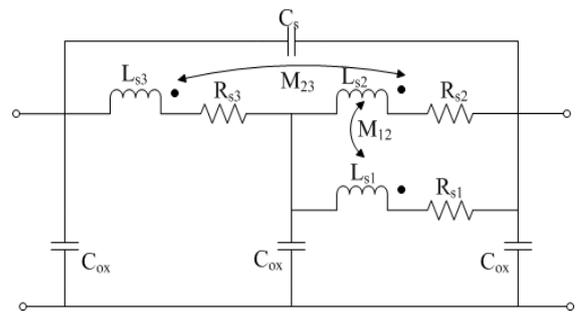


Figure 7 The lumped physical model of the designed stacked inductor

Another obvious parasitic capacitance of this structure is the oxide capacitance C_{ox} between the M1 spiral and the substrate. Its expression is similar to (7),

$$C_{ox} = lw\epsilon_{ox} / t_{ox,1} \quad . \quad (8)$$

$t_{ox,1}$ is the thickness of the SiO_2 layer between M1 and substrate.

Besides C_{ox} , the effects of the silicon substrate resistor R_{si} and substrate capacitor C_{si} in the substrate effect can be neglected in this case because the operating frequency of the spiral inductor which is used in the fully-integrated DC-DC converter is fewer than 500MHz which discussed in the later section.

Synthesize the above analysis, the lumped physical model of the series stacked inductor is shown in Fig.7 and the Q expression is

$$Q = \frac{\omega L_s}{R_s} \cdot \left(1 - \frac{R_s^2 C_{eq}}{L_s} - \omega^2 L_s C_{eq} \right) \quad . \quad (9)$$

And [2]

$$C_{eq} = 1/12 (4C_s + C_{ox}) \quad . \quad (10)$$

C. Strategy of Optimization

For a single-layer spiral inductor, the metal line can be chosen the widest in the permission area to minimize the series resistance. Whereas in the multi-layer spiral, the wider metal width will lead to larger parasitic capacitance which allows the signal to flow directly from the input to output port without passing through the spiral inductor. And from the equations in previous, the coupling capacitance is the key factor depressing the Q value. In a particular CMOS technology, the metal thickness is constant, therefore the metal width w , inner diameter d_{in} and line space s are optimized to get the highest Q in this work.

The different coefficients β and α_i in (4) have been given in [10] for spiral structures of square, hexagonal and octagonal. Hexagonal and octagonal spirals generally occupy higher chip area than square spiral, they are not considered here.

For the square spiral, the coefficients of $\{\beta, \alpha_i\}$ in (4) is $\{0.00162, -1.21, -0.147, 2.40, 1.78, -0.030\}$, and

$$d_{out} = d_{in} + n \cdot w + (n - 1) \cdot s \tag{11}$$

$$\begin{aligned} d_{avg} &= 0.5 \cdot (d_{in} + d_{out}) \\ &= 0.5 \cdot [2d_{in} + n \cdot w + (n - 1) \cdot s] \end{aligned} \tag{12}$$

$$l = (4n + 1) \cdot d_{in} + (4n + 1) \cdot n \cdot (w + s) \tag{13}$$

Substitute (2)-(8) into (9), then Equation (9) becomes the function of the width w , spacing s , inner diameter d_{in} and turn n , and operating frequency f .

and the inductance in unit area L_{unit} is

$$L_{unit} = L_s / d_{out}^2 \tag{14}$$

First, according to the discussion of the relationship between mutual inductance and line-to-line spacing in [12] and the technology used, the value of line spacing s is decided as $2\mu\text{m}$. Then inner diameter d_{in} is supposed as $2w$. So that Q and L_{unit} can be optimized respect to w for $n = \{3, 3.5, 4, 4.5, 5, 5.5, 6\}$. After the metal width w and turns n are confirmed, inner diameter d_{in} is optimized and decided finally.

D. Measurement Results

The designed inductors were fabricated using CMOS 0.5- μm 2P3M mix-signal silicon technology and the detail parameters are given in table I. On-wafer inductors measurements are performed using AV3618A vector network analyzer and micro-manipulator. Wafer and probes are shielded within the probe station during measurement. Short and open de-embedding structures were also fabricated to eliminate the probe and pad parasitics.

The dimension specifications of the four inductors with large inductance from 10nH to 40nH which is necessary to the DC-DC were listed in Table II. They were measured and curves representing the average data are presented here along with model comparisons in Figs. 8-10. Using the model in Fig. 7 and the values from Table I, the simulated model matches well with the inductor measurements across the frequency band.

In the model analysis, we neglected the silicon substrate resistance R_{si} and capacitance C_{si} in the interested frequency band, 50-500MHz. Fig.10 shows the Q factor variation along with the frequency. From it, the Q of the model without considering R_{si} and C_{si} is little higher than the Q of the model considering R_{si} and C_{si} about 2%. And the measurement data match well with the former. Therefore, the designed model can only consider the oxide capacitance C_{ox} of the substrate effects in this frequency range. In addition, the self-resonance decreases with the increasing of the inductance and the self-

TABLE II. DIMENSION SPECIFICATIONS OF THE MEASURED INDUCTORS

	Ind1	Ind2	Ind3	Ind4
$w - \mu\text{m}$	50	70	75	55
$s - \mu\text{m}$	2	2	2	2
$d_{in} - \mu\text{m}$	100	140	150	110
n	3	3.5	4	5
Calculated $L_s - \text{nH}$	10.3	21.5	31.1	39.1

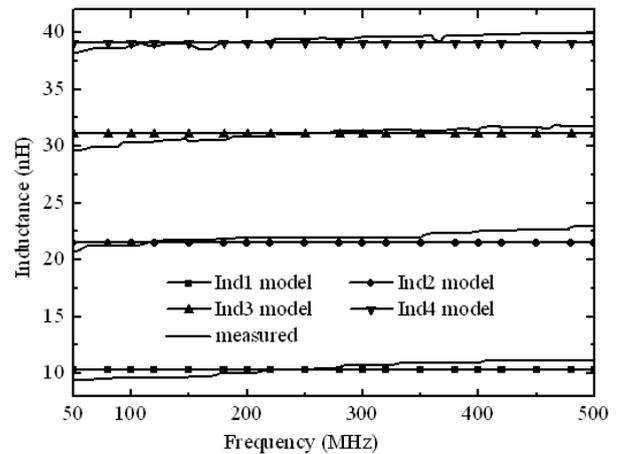


Figure 8. Inductance of the measured inductors

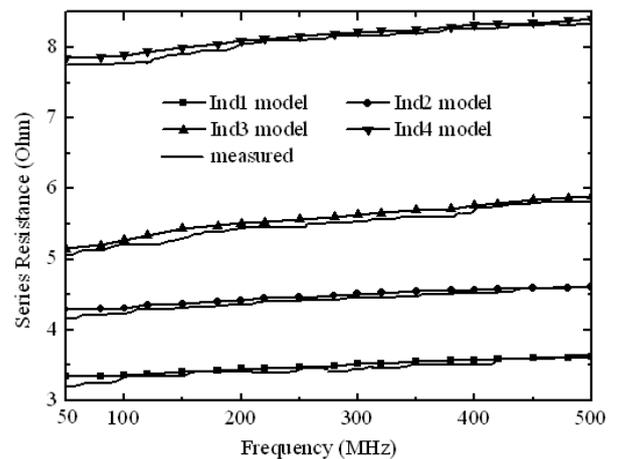
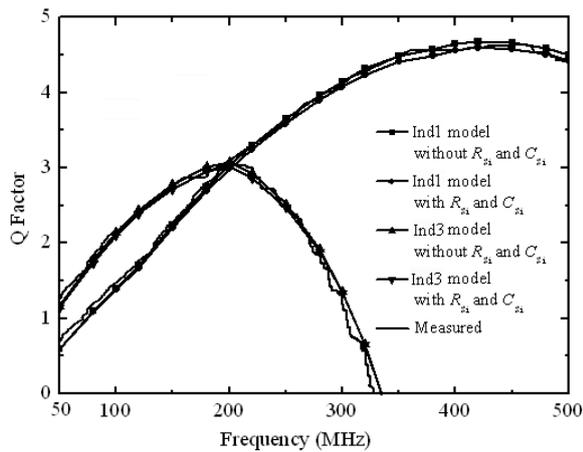
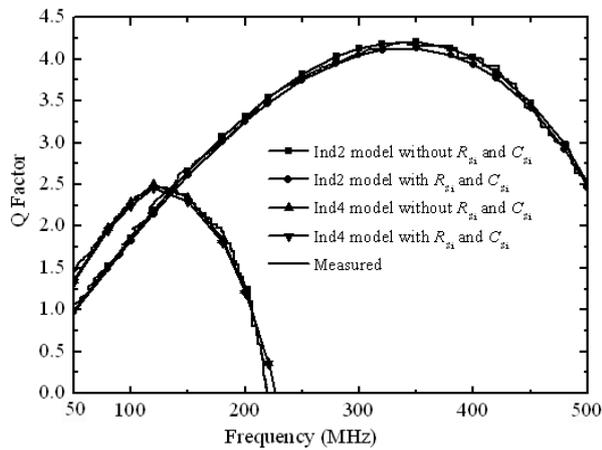


Figure 9. Resistance of the measured inductors

resonance of the designed structure is not high because of the large series capacitance caused by the series branch. However, the performance of the designed inductor can satisfy the demand of the DC-DC converter.



(a)



(b)

Figure 10. Q variation of the designed structure versus frequency

IV. MEASUREMENT RESULTS OF BUCK CONVERTER

The designed fully-integrated 5V-2.5V buck converter was fabricated using CMOS 0.5- μm 2P3M mix-signal silicon technology. Its detail parameters are given in Table III. The desired on-chip inductor is Ind4 in Table II. On-wafer measurements are performed using Tek TDS3012B oscillograph and micro-manipulator. Wafer and probes are shielded within the probe station during measurement.

Fig. 11 is the measurement results of input and output voltage at the load of 22 Ω . With the steady input voltage of 5V, the average output voltage of the converter is 2.45V.

Fig. 12 is the Measured waveform of Output voltage ripple ΔV_{out} . From the result, the maximum peak-to-peak value of ΔV_{out} is 50mV. Then the output voltage ripple can be controlled in $\pm 2\%$.

TABLE III. SPECIFICATIONS OF THE MEASURED FULLY-INTEGRATED BUCK CONVERTER

L_f (nH)	C_f (nF)	f_s (MHz)
40	5	100

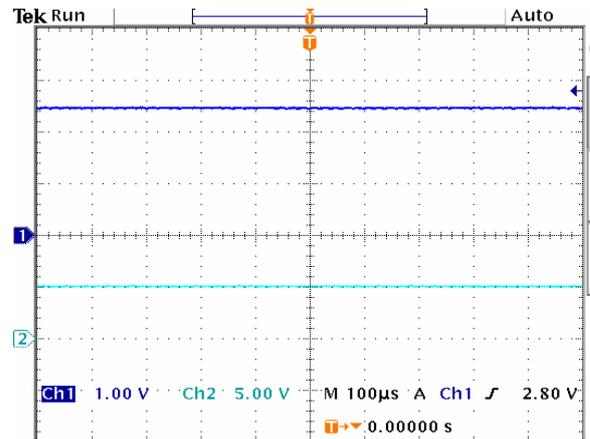


Figure 11. Measurement result of input and output voltage

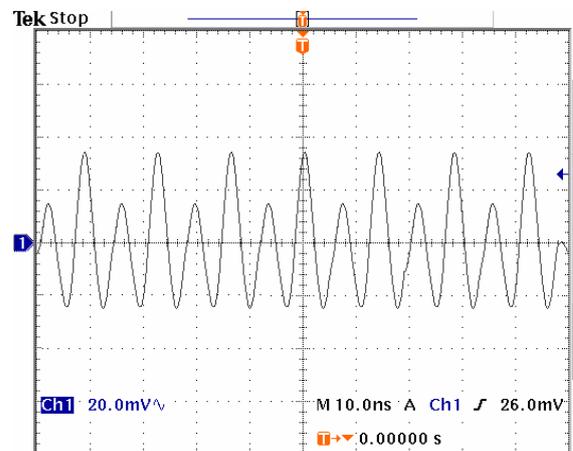
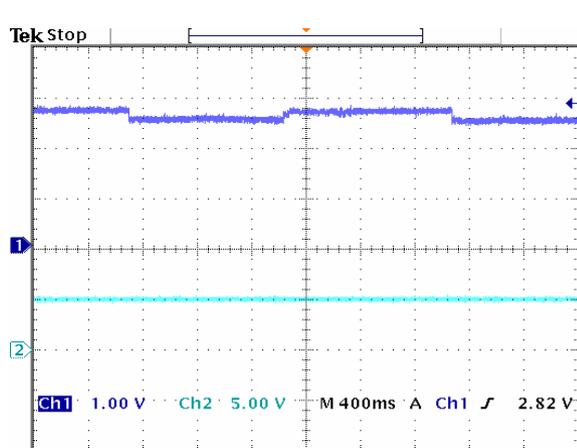


Figure 12. Measured Output voltage ripple waveform.

Fig.13 is the output voltage waveform varied with the different load of 50 Ω and 35 Ω . The other conditions such as input voltage of 5V are constant. From the result, the average output voltage of the converter is 2.6V with the load of 35 Ω and 2.8V with the load of 50 Ω . From Fig. 11, the average output voltage of the converter is 2.45V with the load of 22 Ω . The average output voltage of the converter is variable with different load conditions. The load's modulation of the converter is -12dB with the load varied from 10 Ω to 60 Ω .



(a)

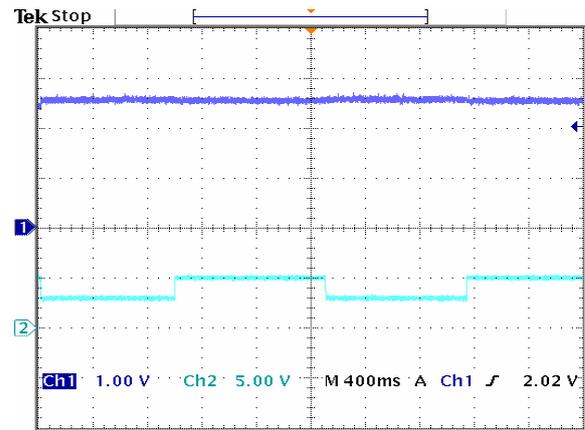
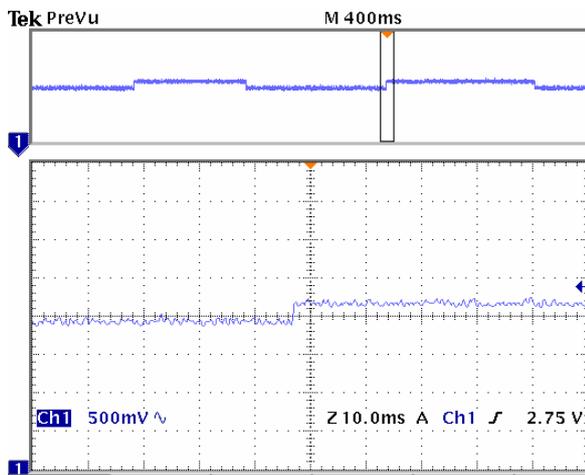


Figure 14. Output voltage with the varied input voltage.



(b)

Figure 13. The output voltage with the varied load. (a) global; (b) microscope.

Fig. 14 is the output voltage waveform varied with the different input voltage. The average output voltage of the converter is almost constant when the input voltage varied from 3V to 5V. The voltage modulation of the fully-integrated converter is -40dB with the input voltage varied from 3V to 5V.

The efficiency of the integrated converter is

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \quad (15)$$

For an output voltage of 2.5V at 100mA, $\eta = 46\%$.

V. CONCLUSIONS

This paper presented an optimum design of fully-integrated low-power buck converter with on-chip components. As an example, a 5V to 2.5V buck converter operating at 100MHz was designed and implemented using 0.5 μ m standard CMOS technology. The key circuits in the controller block operating at high frequency are described, and the series parallel stacked spiral inductors are designed and optimized in this paper. It was found that there are many restrictions in designing passive components. Especially, parasitic capacitance and current capability are critical restrictions. In this structure, the parallel branch decreases the series resistance with the increased effective metal thickness and the series branch increases the mutual inductance between spirals. The self-resonance of the designed structure is not high, but it can satisfy the demand of the fully-integrated DC-DC. Based on the analysis of the physical mechanism, the scalable lumped model was given, which can provide effective simulation of the fully-integrated DC-DC converter system. From the measurement results, the whole converter system can operate stably. At the same time, the efficiency of 46% is achieved. The efficiency of the converter still is lower, further optimization should be done in design.

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